Investigation on 15-Level Asymmetric Multilevel Inverter with Reduced Switch Count Using Carrier Shift PWM Technique

Uppala Sivamani[1], Kemburi Raju[2], Kuppala Mohan sai[3], Devarakonda Gopichand[4], Kaladhar Gaddala[5]
[1,2,3,4]UG Scholar,[5A]ssociate Professor
Department of Electrical and Electronics Engineering, St.Ann's College of Engineering and Technology,Chirala, India
Email id : sivamaniuppala63@gmail.com[1], rajukemburi2004@gmail.com[2], sainaidu0085 @gmail.com, alladi_007@yahoo.com[3], Venkatgopisurendradevarakona@gmail.com[5]

Article Received: 29 May 2025 *Article Accepted: 15 June 2025* *Article Published: 10 July 2025*

Citation
Uppala Rivamani, Kemburi Raju, Kuppala Mohan sai, Devarakonda Gopichand, Kaladhar Gaddala, "Investigation on 15-Level Asymmetric Multilevel Inverter with Reduced Switch Count Using Carrier Shift PWM Technique", Journal of Next Generation Technology (ISSN: 2583-021X), 5(5), pp. 75-84. July 2025. DOI: 10.5281/zenodo.16787959

Abstract

Asymmetric multilevel inverters (AMLIs) are increasingly adopted in medium-voltage and high-power systems due to their ability to produce high-resolution voltage waveforms with lower harmonic content and reduced electromagnetic emissions. This study introduces a novel 15-level AMLI architecture designed to minimize the number of power switches and passive components, thereby enhancing system efficiency and reducing overall cost. The inverter employs unequal DC voltage sources and is capable of operating in multiple switching states to efficiently generate the required voltage levels. To evaluate the output waveform quality and harmonic performance, the proposed design is tested using various pulse-width modulation (PWM) strategies, including Level-Shifted PWM (LSPWM), Sinusoidal PWM (SPWM), and Selective Harmonic Elimination PWM (SHE-PWM). Simulation results obtained in MATLAB/Simulink confirm that the inverter delivers high-quality output with low total harmonic distortion (THD), demonstrating its suitability for industrial applications and renewable energy integration where efficiency and power quality are critical.

Keywords: Asymmetric multilevel inverter, reduced switch count, PWM techniques, total harmonic distortion (THD), MATLAB/Simulink, high-quality waveform, power electronics.

I. Introduction

Multilevel inverters (MLIs) have emerged as a crucial technology in medium-voltage and high-power applications due to their superior output waveform quality, reduced electromagnetic interference, and higher efficiency compared to conventional two-level inverters [1], [2]. These features make MLIs particularly well-suited for use in electric vehicles, industrial motor drives, and renewable energy systems [3], [4]. Among the various MLI topologies, the asymmetric multilevel inverter (AMLI) is especially notable for its ability to generate a greater number of voltage levels while utilizing fewer power electronic components. This is achieved by employing DC voltage sources of unequal magnitudes, typically configured in binary or trinary ratios [5], [6]. Such an arrangement simplifies circuit design, reduces hardware complexity, and lowers the overall system cost [7].

Recent advancements have focused on AMLI topologies that reduce the number of power switches required, aiming to further improve system efficiency, reliability, and compactness [8], [9]. A critical performance metric in MLI design is the total harmonic distortion (THD) of the output voltage waveform, as lower THD directly contributes to reduced power losses, improved system efficiency, and extended lifespan of connected equipment. To mitigate THD, a variety of pulse-width modulation (PWM) techniques have been explored, including level-shifted PWM (LSPWM), selective harmonic elimination PWM (SHE-PWM), and sinusoidal PWM (SPWM) [10]–[12]. Each modulation strategy offers specific trade-offs in terms of harmonic suppression capability, control complexity, and switching loss [13].

The development of a 15-level AMLI with a minimized switch count presents an attractive solution for generating high-fidelity output waveforms while maintaining a compact and efficient system design [14], [15]. Integrating advanced PWM schemes into such a topology can further enhance inverter performance, making it highly applicable in modern power electronics applications[16]-[18].

In this context, the primary objective of this study is to design and analyze a 15-level AMLI that employs non-uniform DC voltage sources and a reduced number of switches. The inverter's performance is evaluated based on output voltage quality, efficiency, and THD under different PWM strategies. Simulation results, conducted in the MATLAB/Simulink environment, validate the proposed design's effectiveness and demonstrate its suitability for use in industrial motor drives and renewable energy systems.

II. System Description

The schematic of the proposed converter is illustrated in Figure 1. This topology employs DC voltage sources of varying magnitudes—typically arranged in binary (e.g., 1:2:4) or trinary (e.g., 1:3:9) ratios—to achieve a higher number of output voltage levels with a reduced component count. Unlike symmetric multilevel inverter configurations that require equal DC sources and a larger number of switches to increase levels, the asymmetric approach enables a significant increase in output levels without proportionally increasing the number of power switches. By leveraging unequal voltage sources, Asymmetric Multilevel Inverters

(AMLIs) present an efficient means of synthesizing high-resolution output waveforms. This configuration effectively lowers total harmonic distortion (THD), making it well-suited for applications demanding superior power quality and reduced switching complexity.

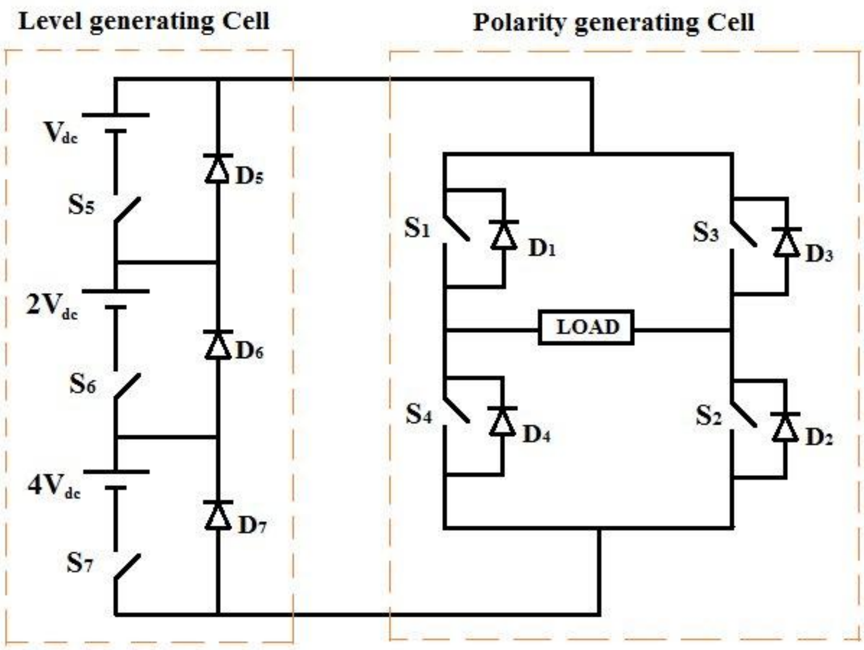


Figure 1: Circuit diagram of proposed 15 level converter

One of the primary benefits of using AMLIs is the reduced number of semiconductor switches and associated driver circuits. This simplification leads to lower switching losses, decreased system complexity, and enhanced overall efficiency. Due to these characteristics, AMLIs are increasingly employed in areas requiring reliable and high-performance power conversion, such as renewable energy integration, electric mobility, industrial automation, and smart grid systems. The ability to achieve multiple voltage steps without proportionally increasing the number of switches is made possible through strategic voltage scaling. This involves using unequal DC voltage levels that are mathematically optimized to maximize the number of output levels. Configurations may follow binary, trinary, or other asymmetric sequences depending on design requirements.

Finding the ideal DC voltage levels and modulation technique to preserve output voltage balance and accomplish effective switching is a major design issue. Space vector modulation (SVM), selective harmonic elimination (SHE-PWM), and sinusoidal pulse width modulation (SPWM) are often employed modulation techniques.These techniques are instrumental in improving waveform quality and minimizing harmonic components. To enhance system robustness, especially in demanding applications, fault-tolerant inverter designs are being explored. Such approaches aim to maintain stable operation under fault conditions, ensuring reliability and continuity in critical systems. Due to their excellent harmonic performance, energy efficiency, and compact structure, AMLIs continue to replace traditional two-level and symmetric multilevel inverters in many high-power applications. Continued research is being directed toward the development of novel AMLI topologies, advanced control algorithms, and hybrid systems. These innovations aim to further reduce component count, increase modulation flexibility, and expand the usability of AMLIs in future-oriented energy conversion platforms.

For an *m-level inverter*, the number of carriers required is:

$N_c = m - 1$

$For\ a\ 15 - level\ MLI$:

$Nc = 15 - 1 = 14$

Let the **carrier signals** $c_i(t)$ be defined as:

$c_i(t) = A_c \cdot \text{triangular}(f_c, \phi_i), \quad i = 1,2, \ldots ,14$

Where:

- A_c is the peak amplitude of the carrier
- f_c is the carrier frequency
- ϕ_i is the phase shift or offset for the i^{th}carrier

Each carrier is a triangular waveform:

$$Ci(t) = Ac \cdot triangular(fc \cdot t) + (i - 1) \cdot \Delta VC_i(t)$$

The sinusoidal modulating reference signal is:

$$Vref(t) = Am \cdot si\,n(2\pi fmt)$$

The output level of the inverter is determined by counting how many carrier signals the reference surpasses:

Let the **switching logic** be defined as:

$$S(t) = \sum_{i=1}^{N_c} u\left(V_{ref}(t) - C_i(t)\right)$$

Where:

- $u(x)$ is the unit step function:

$$u(x) = \{1, x \geq 0$$
$$0, x < 0\}$$

Thus:

Output level=S(t)

For **symmetric configuration** with identical DC sources:

$$Vo(t) = S(t) \cdot Vdc$$

This equation simply counts how many carriers the reference has crossed, which directly determines the instantaneous output voltage level.

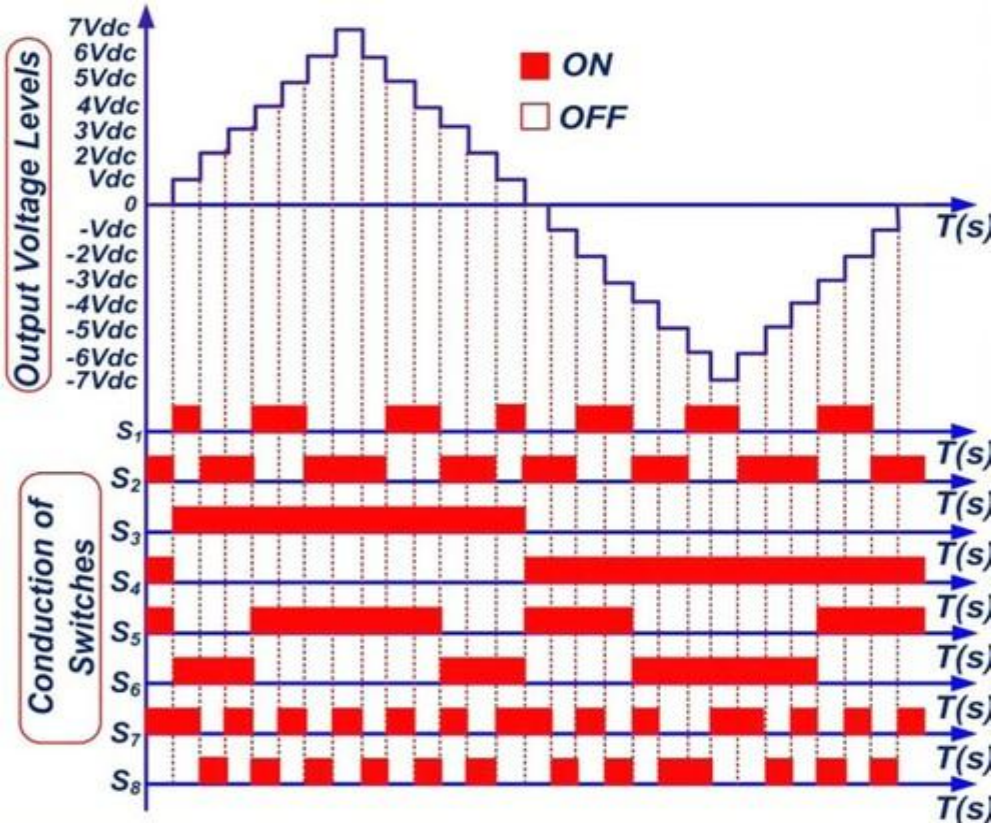


Figure 2 : Switching angles for the conduction of switches

III. Control Logic of Proposed 15 Level MLI

The proposed 15 Level MLI output is obtained by feeding it with appropriate switching angles generated by comparing the level shifted carrier signals with reference signal . Totally there were seven outputs from the seven comparators and these are used in such a way to generate three switching pulses required to fire upper commutation group switches

The H- bridge inverter is used to flip the obtained half cycle after 180 degrees to obtain complete 15 level MLI output waveform at the converter output.

IV. RESULTS & DISCUSSION

The proposed system's Simulink diagram is shown below.

The 15 level MLI carrier and reference signals and half wave output is as shown in Figure 4. Here the 7 comparator is identified the difference between respective carrier and reference sine wave and the output is obtained in the form of c1 to c7 which is fed to control logic to generate s1 to s3 to operate 15 level MLI . represents the output waveform of a 15-level asymmetric multilevel inverter simulated using

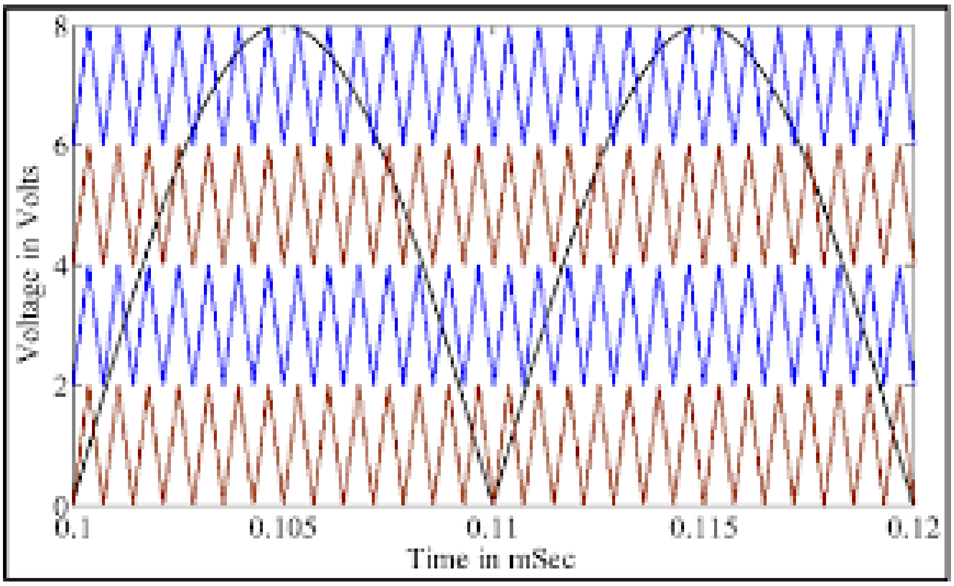


Figure 3: Simulink implementation of 15 level MLI to generate a half wave.

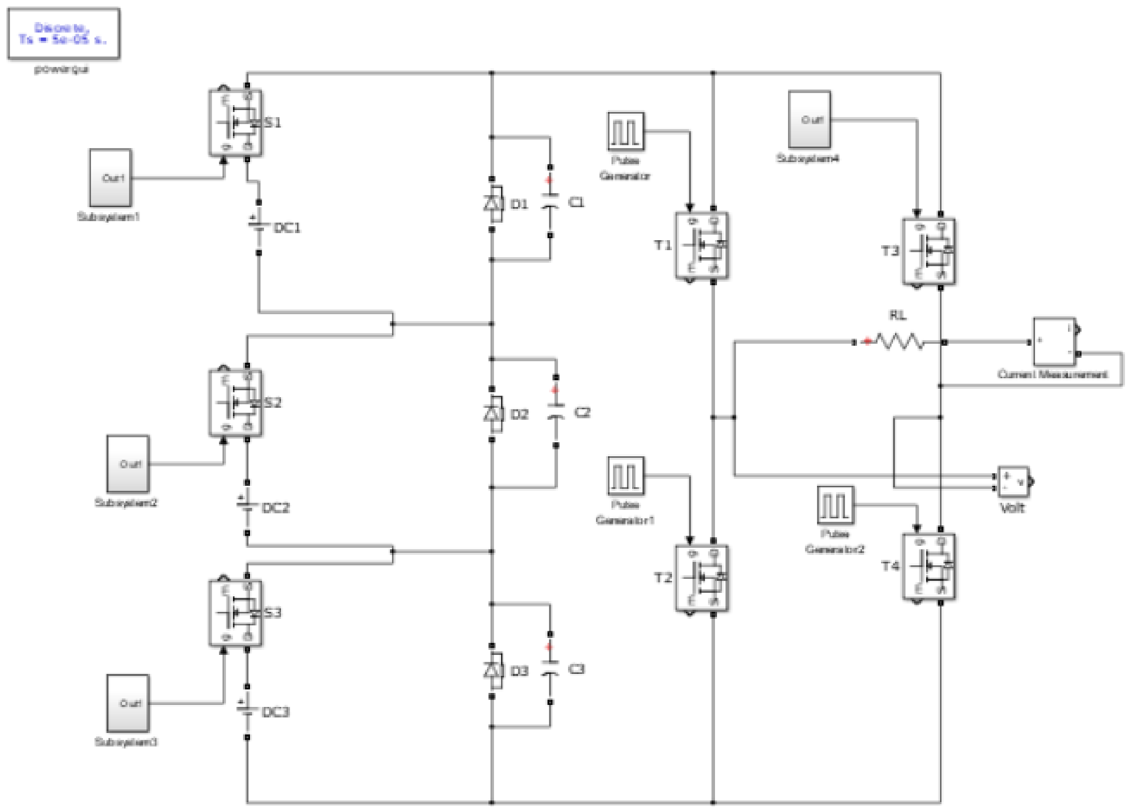
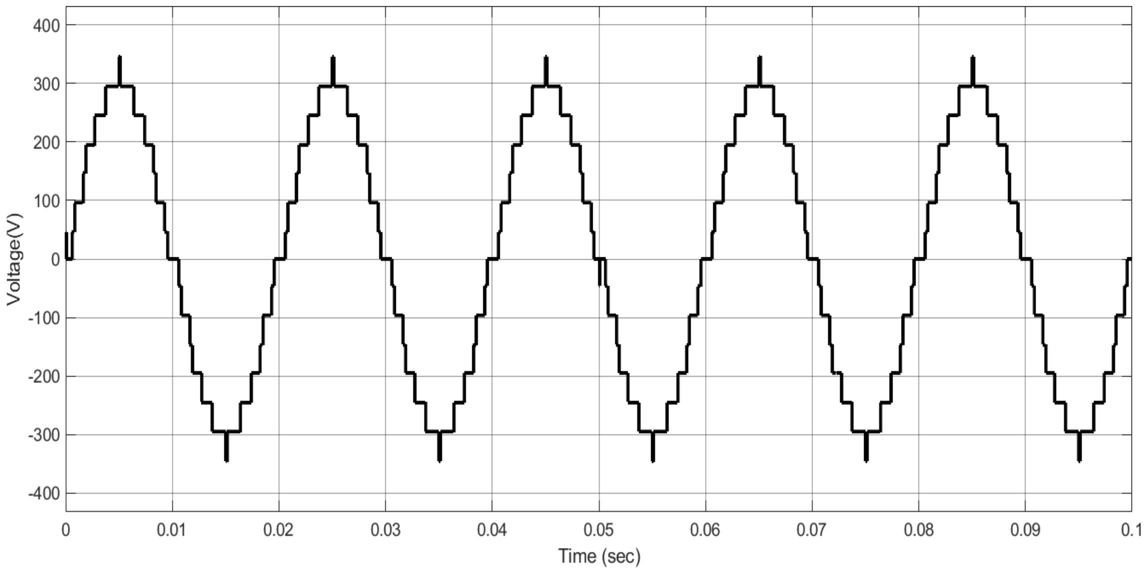


Figure 4: Simulink implementation of 15 level MLI to generate a half wave.

Figure 6: Carrier and reference waves for generation of 15 Level voltage output.



.

Figure5: 15 Level MLI output voltage waveform

MATLAB/Simulink. The inverter is powered by three unequal DC sources with voltages 50 V, 100 V, and 200 V, configured in a 1:2:4 ratio. This asymmetric configuration is chosen to optimize the number of levels with fewer switches and reduce power losses. By combining these voltages in various ways using controlled switching, the inverter is able to produce fifteen distinct output levels, ranging from –350 V to +350 V in symmetrical steps. These levels include: ±50 V, ±100 V, ±150 V, ±200 V, ±250 V, ±300 V, ±350 V, and 0 V. The resulting waveform is a staircase approximation of a sinusoidal signal, and the high number of steps leads to reduced voltage stress on the components and minimal harmonic content. The modulation technique used is Carrier Shifted Pulse Width Modulation (CSPWM),

which ensures balanced switching and better harmonic suppression.

A pure resistive load of 300 ohms is connected at the inverter output. The use of a resistive load allows for accurate waveform analysis since the current follows the same shape as the voltage without any phase shift. The load ensures linear response and helps in clearly observing the voltage steps generated by the inverter.

The Total Harmonic Distortion (THD) calculated from the simulation is approximately 3.57%, which is significantly lower than conventional two-level inverters. This low THD value implies improved power quality and compatibility with sensitive AC loads, and it meets the IEEE 519 standard for harmonic limits in power systems.

Overall, the simulation validates the effectiveness of the designed inverter topology in producing high-quality output with fewer components and reduced switching losses, making it suitable for medium-voltage and renewable energy applications.

ANALYSIS:

S.NO	PWM TECHNIQUE	THD%
1	PDPWM	8.98
2	PODPWM	9.42
3	APODPWM	9.03
4	HYBRID PWM	9.15
5	PHASE SHIFTED PWM	9.14
6	CARRIER SHIFT PWM	5 to 15

V. Conclusion

The proposed 15-level asymmetric multilevel inverter (AMLI) topology, incorporating only 7 switches, 3 diodes, and 3 DC link capacitors, offers a highly optimized solution for medium- to high-voltage applications. By leveraging Carrier Shifted PWM (CSPWM), the system efficiently synthesizes 15 voltage levels with a minimal number of components, significantly reducing cost, control complexity, and switching losses. The asymmetric configuration allows for unequal DC voltage sources, enhancing output waveform resolution and reducing total harmonic distortion (THD). The CSPWM technique ensures superior harmonic performance through the use of phase-shifted triangular carriers, enabling cleaner AC waveforms with consistent switching frequency and improved power quality. This approach not only enhances efficiency but also prolongs inverter lifespan by mitigating thermal and switching stresses.

With its compact structure and scalable nature, the inverter is well-suited for a broad spectrum of applications, including renewable energy systems, electric vehicle drives, and smart grid-connected converters. Overall, the design demonstrates a compelling balance between performance, modularity, and economic viability, making it a strong candidate for future high-efficiency power conversion systems

References

[1]. J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2]. B. Wu, *High-Power Converters and AC Drives*, Wiley-IEEE Press, 2006.

[3]. L. G. Franquelo et al., "The age of multilevel converters begins," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[4]. N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[5]. S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[6]. M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[7]. E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[8]. H. R. Mohammadi, A. Y. Varjani, and H. R. Toodeji, "Multilevel inverter topologies for electric drives: A review," *Renewable and Sustainable Energy Reviews*, vol. 24, pp. 569–578, Aug. 2013.

[9]. S. Khomfoi and L. M. Tolbert, "Multilevel power converters," in *Power Electronics Handbook*, 2nd ed., Elsevier, 2007, pp. 451–482.

[10]. D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, Wiley-IEEE Press, 2003.ResearchGate
[11]. J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 491–499, Mar. 2004.
[12]. J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE*, vol. 82, no. 8, pp. 1194–1214, Aug. 1994.
[13]. M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1620–1630, Jul. 2008.
[14]. E. Najafi and A. H. M. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 11, pp. 4148–4154, Nov. 2012.
[15]. R. Stala, "The switch-mode flying-capacitor DC–DC converters with improved natural balancing," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 554–564, Feb. 2013.
[16]. Paramasivan, M., Prasad, T.N. & Vanchinathan, K. Experimental and numerical investigations on amalgamation of mixed frequency carrier based asymmetrical 15 level multilevel inverter. Electr Eng 107, 5861–5875 (2025). https://doi.org/10.1007/s00202-024-02854-2
[17]. P. Muthukumar, S. A. Raj, T. N. Prasad, S. Nageswari, J. T and K. Eswaramoorthy, "Design and Analysis of Photovoltaic System Based Single Phase Multilevel Inverter with Grid Integration," 2024 International Conference on Advancement in Renewable Energy and Intelligent Systems (AREIS), Thrissur, India, 2024, pp. 1-5, doi: 10.1109/AREIS62559.2024.10893622.
[18]. Gavini Ayyappa, Deverakonda Srikanth, Kesana Trivikram, Kommanaboina Siva Koteswararao, K. Naveen Babu, “Bi-directional DC /AC and DC / DC converter design and control for plug-in hybrid cars”, Journal of Next Generation Technology (ISSN: 2583-021X), 5(1), pp. 42-51. March 2025. https://doi.org/10.5281/zenodo.15250278